1.5A, 15V Monolithic Synchronous Step-Down Regulator

FEATURES

- **4V to 15V Operating Input Voltage Range**
- **1.5A Output Current**
- **Up to 96% Efficiency**
- **Very Low Duty Cycle Operation: 5% at 2.25MHz**
- **Adjustable Switching Frequency: 800kHz to 4MHz**
- **External Frequency Synchronization**
- **Current Mode Operation for Excellent Line and Load Transient Response**
- User Selectable Burst Mode® (No Load I_Q = 300µA) or Forced Continuous Operation
- 0.6V Reference Allows Low Output Voltages
- Short-Circuit Protected
- Output Voltage Tracking Capability
- Programmable Soft-Start
- Power Good Status Output
- Available in Small, Thermally Enhanced 16-Pin QFN (3mm × 3mm) and MSOP Packages

APPLICATIONS

- Distributed Power Systems
- Lithium-Ion Battery-Powered Instruments
- Point-of-Load Power Supply

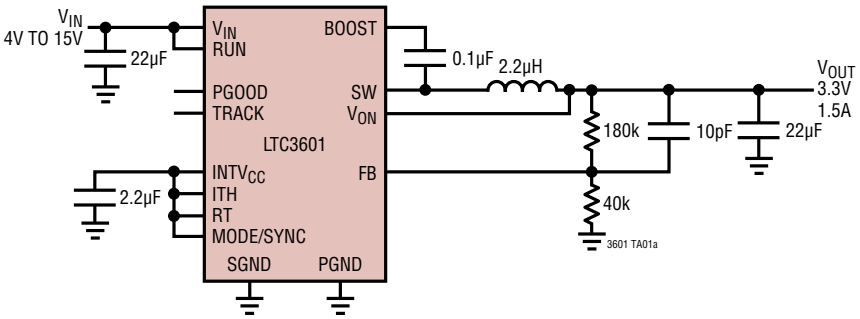
DESCRIPTION

The LTC®3601 is a high efficiency, monolithic synchronous buck regulator using a phase-lockable controlled on-time, current mode architecture capable of supplying up to 1.5A of output current. The operating supply voltage range is from 4V to 15V, making it suitable for a wide range of power supply applications.

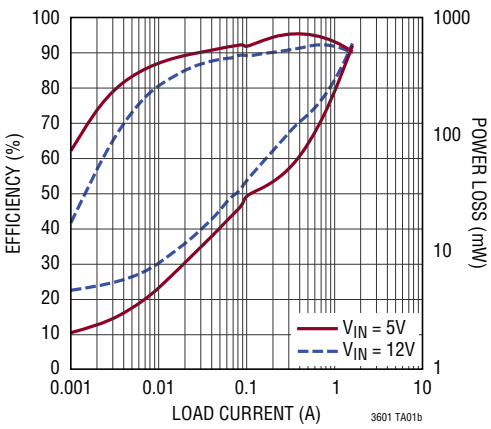
The operating frequency is programmable from 800kHz to 4MHz with an external resistor enabling the use of small surface mount inductors. For switching noise sensitive applications, the LTC3601 can be externally synchronized over the same frequency range. An internal phase-locked loop aligns the on-time of the top power MOSFET to the internal or external clock. This unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that demand high switching frequencies and fast transient response.

The LTC3601 offers two operational modes: Burst Mode operation and forced continuous mode to allow the user to optimize output voltage ripple, noise, and light load efficiency for a given application. Maximum light load efficiency is achieved with the selection of Burst Mode operation while forced continuous mode provides minimum output ripple and constant frequency operation.

TYPICAL APPLICATION



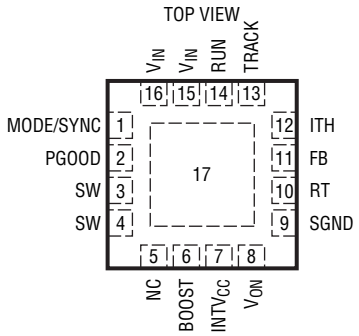
Efficiency and Power Loss vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

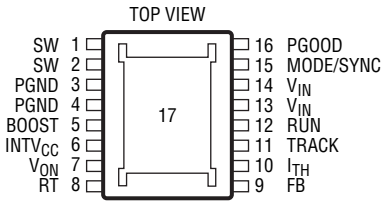
V_{IN} ..... –0.3V to 16V
V_{IN} Transient Voltage 18V
BOOST ..... –0.3V to 18.6V
BOOST-SW ..... –0.3V to 3.6V
$INTV_{CC}$ ..... –0.3V to 3.6V
ITH, RT ..... –0.3V to $INTV_{CC}$ + 0.3V
MODE/SYNC, FB ..... –0.3V to $INTV_{CC}$ + 0.3V
TRACK ..... –0.3V to $INTV_{CC}$ + 0.3V
PGOOD, V_{ON} ..... –0.3V to 16V
SW, RUN ..... –0.3V to V_{IN} + 0.3V
SW Source Current (DC) 2A
Peak SW Source Current 3.5A
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3601EUD#PBF	LTC3601EUD#TRPBF	LFJC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3601IUD#PBF	LTC3601IUD#TRPBF	LFJC	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3601EMSE#PBF	LTC3601EMSE#TRPBF	3601	16-Lead Plastic MSOP	–40°C to 125°C
LTC3601IMSE#PBF	LTC3601IMSE#TRPBF	3601	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{VIN} = 12V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{VIN}	Input Supply Range		●	4		15	V
I_Q	Input DC Supply Current Forced Continuous Operation Sleep Current Shutdown	 MODE = 0V MODE = $INTV_{CC}$, V_{FB} > 0.6V RUN = 0V			 700 300 14	 1000 500 25	 µA µA µA
V_{FB}	Feedback Reference Voltage		●	0.594	0.600	0.606	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{VIN} = 4V to 15V			0.01		%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	ITH = 0.6V to 1.6V			0.1		%
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.6V				±30	nA
$g_{m(EA)}$	Error Amplifier Transconductance	ITH = 1.2V			2.0		mS
$t_{ON(MIN)}$	Minimum On-Time	V_{ON} = 1V, V_{IN} = 4V			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	V_{IN} = 6V			40	60	ns
I_{LIM}	Valley Switch Current Limit			1.7	2.2	2.8	A
	Negative Valley Switch Current Limit				–1.2		A
f_{OSC}	Oscillator Frequency	V_{RT} = $INTV_{CC}$ R_{RT} = 160k R_{RT} = 80k		1.4 1.7 3.4	2 2 4	2.6 2.3 4.6	MHz MHz MHz
$R_{DS(ON)}$	Top Switch On-Resistance				130		mΩ
	Bottom Switch On-Resistance				100		mΩ
V_{VIN-OV}	V_{IN} Overvoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling	● ●	16.8 15.8	17.5 16.5	18 17	V V
V_{INTVCC}	$INTV_{CC}$ Voltage	4V < V_{IN} < 15V		3.15	3.3	3.45	V
$\Delta INTV_{CC}$	$INTV_{CC}$ Load Regulation (Note 4)	I_{INTVCC} = 0mA to 20mA			0.6		%
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising, V_{IN} = $INTV_{CC}$ $INTV_{CC}$ Falling, V_{IN} = $INTV_{CC}$			2.75 2.45	2.9	V V
V_{RUN}	RUN Threshold	RUN Rising RUN Falling	● ●	1.21 0.97	1.25 1.0	1.29 1.03	V V
$I_{RUN(LKG)}$	RUN Leakage Current	V_{VIN} = 15V			0	±3	µA
V_{FB_GB}	PGOOD Good-to-Bad Threshold	FB Rising FB Falling			8 –8	10 –10	% %
V_{FB_BG}	PGOOD Bad-to-Good Threshold	FB Rising FB Falling		–3 3	–5 5		% %
t_{PGOOD}	Power Good Filter Time			20	40		µs
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			15		Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{RUN} = 0V			0.01	1	µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 10% to 90% Full Scale			400	700	µs
V_{FB_TRACK}	TRACK Pin	TRACK = 0.3V		0.28	0.3	0.315	V
I_{TRACK}	TRACK Pull-Up Current				1.4		µA
$V_{MODE/SYNC}$	MODE Threshold Voltage	MODE V_{IH} MODE V_{IL}	● ●	1.0		 0.4	V V
	SYNC Threshold Voltage	SYNC V_{IH}	●	0.95			V
I_{MODE}	MODE Input Current	MODE = 0V MODE = $INTV_{CC}$			–1.5 1.5		µA µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3601 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3601E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3601I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

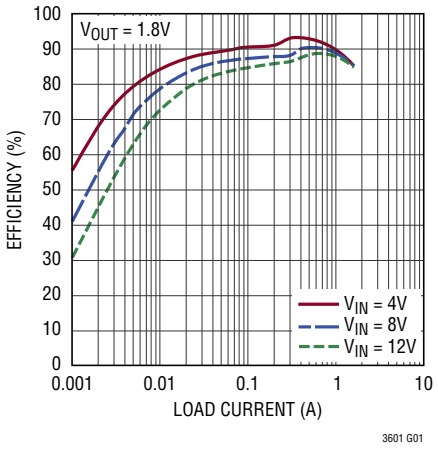
where θ_{JA} = 45°C/W for the QFN package and θ_{JA} = 38°C/W for the MSOP package.

Note 4: Maximum allowed current draw when used as a regulated output is 5mA. This supply is only intended to provide additional DC load current as needed and not intended to regulate large transient or AC behavior as these waveforms may impact LTC3601 operation.

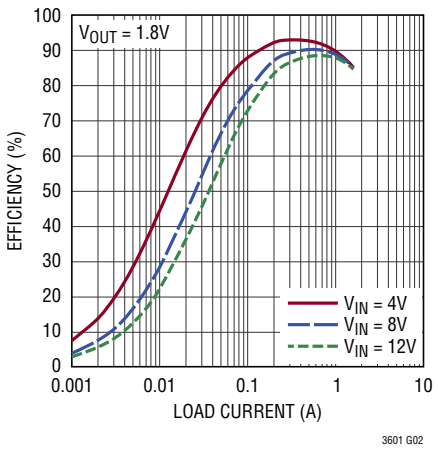
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_O = 1MHz, L = 2.2µH unless otherwise noted.

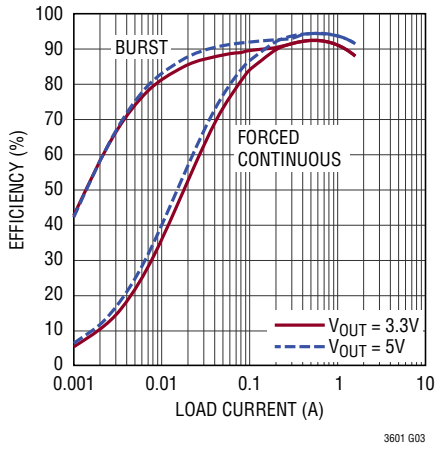
Efficiency vs Load Current Burst Mode Operation



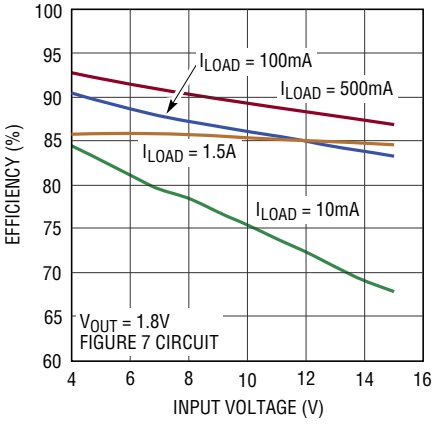
Efficiency vs Load Current Forced Continuous Mode



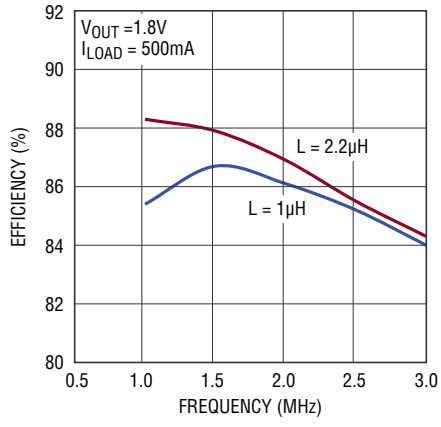
Efficiency vs Load Current



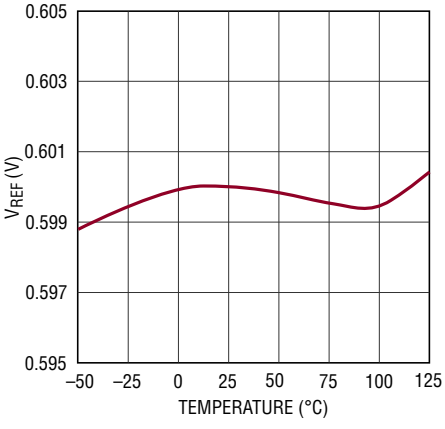
Efficiency vs Input Voltage Burst Mode Operation



Efficiency vs Frequency Forced Continuous Mode



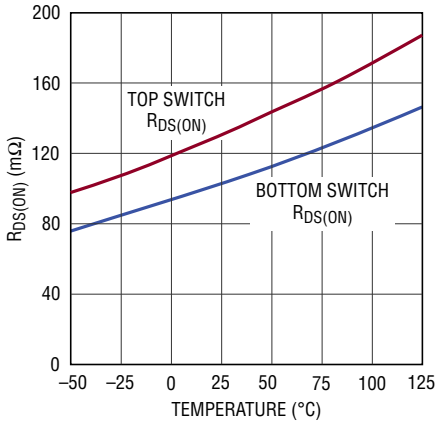
Reference Voltage vs Temperature



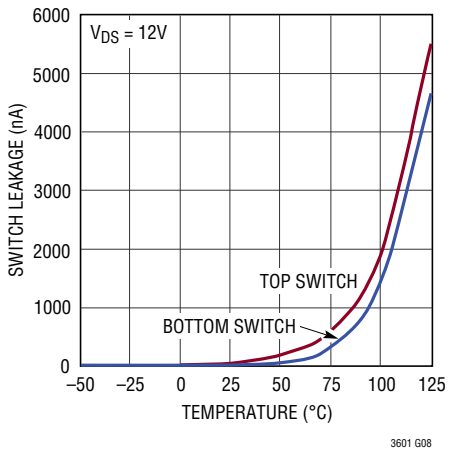
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_O = 1MHz, L = 2.2µH unless otherwise noted.

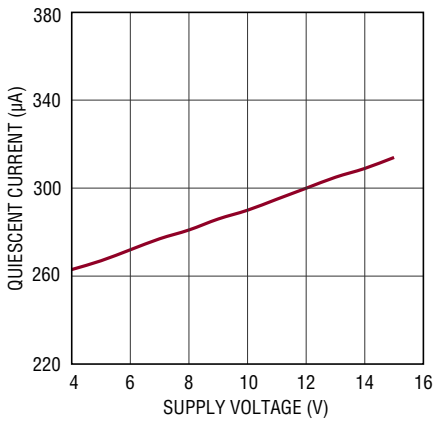
$R_{DS(ON)}$ vs Temperature



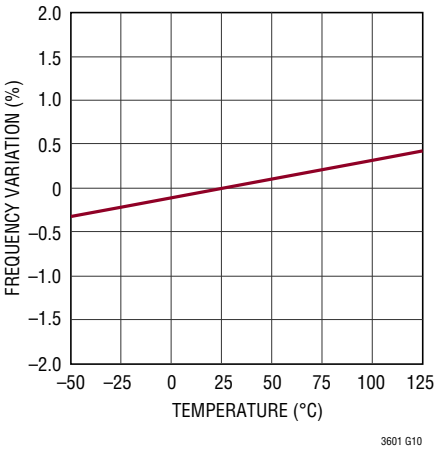
Switch Leakage vs Temperature



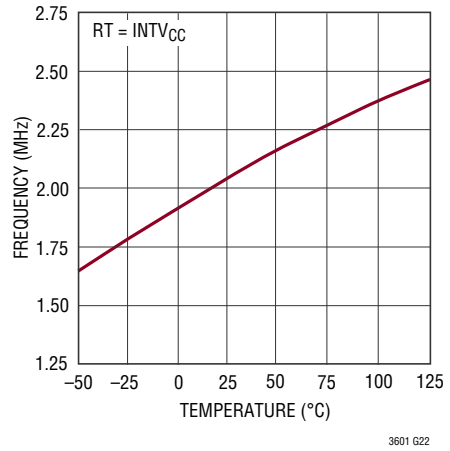
Quiescent Current vs Supply Voltage



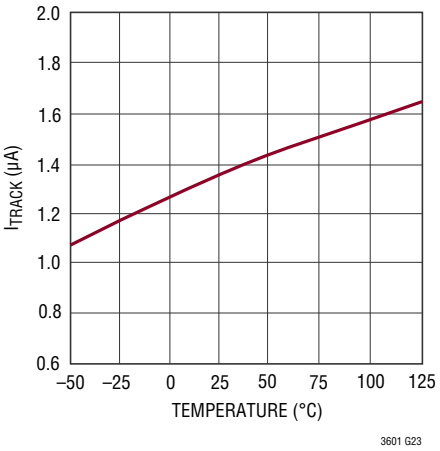
Oscillator Frequency vs Temperature



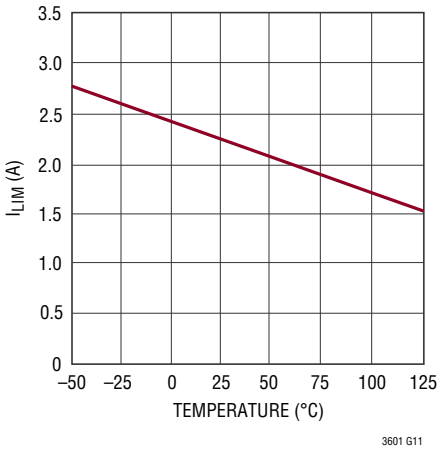
Oscillator Internal Set Frequency vs Temperature



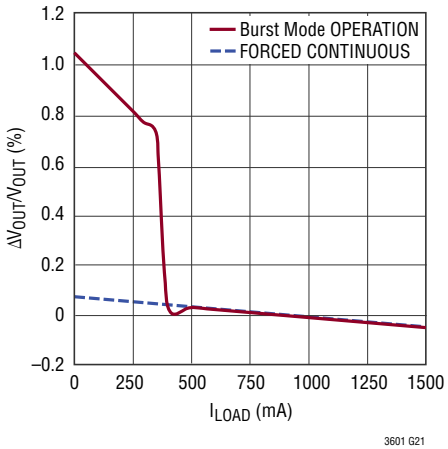
TRACK Pull-Up Current vs Temperature



Bottom Switch Current Limit vs Temperature



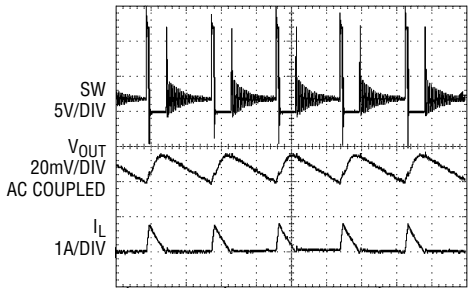
Load Regulation



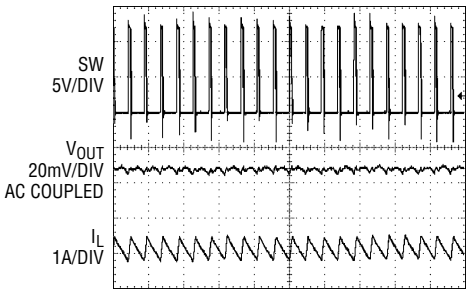
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, f_O = 1MHz, L = 2.2µH unless otherwise noted.

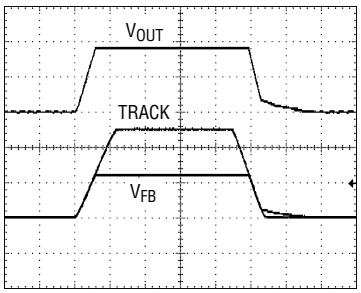
Output Voltage vs Time Burst Mode Operation



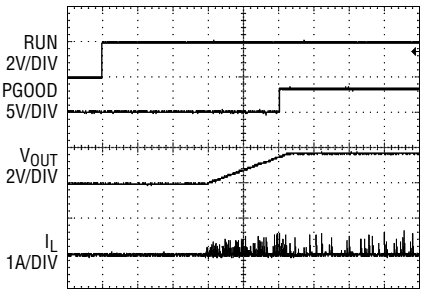
Output Voltage vs Time Forced Continuous Mode



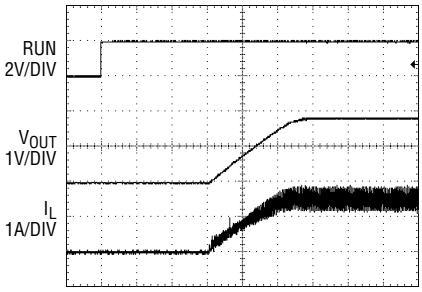
Output Tracking



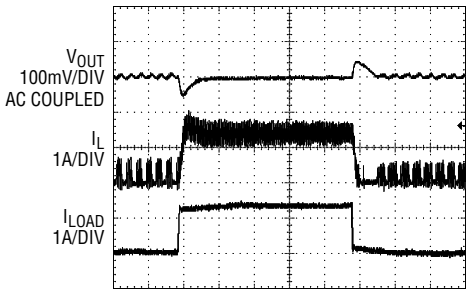
Start-Up from Shutdown Burst Mode Operation



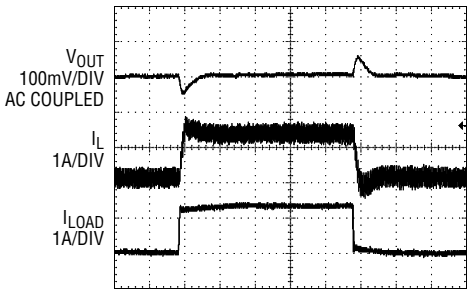
Start-Up from Shutdown Forced Continuous Mode



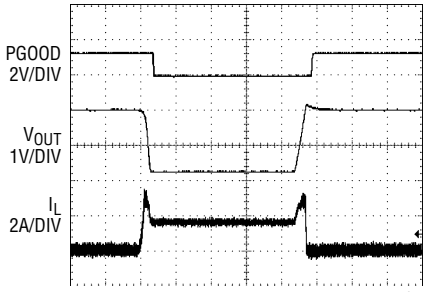
Load Step Burst Mode Operation



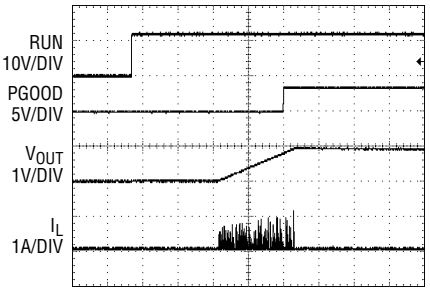
Load Step Forced Continuous Mode



Short-Circuit Waveforms Forced Continuous Mode



Start-Up Into Pre-Biased Output (1V Pre-Bias) Burst Mode Operation



PIN FUNCTIONS (QFN/MSE)

MODE/SYNC (Pin 1/Pin 15): Mode Selection and External Synchronization Input Pin. This pin places the LTC3601 into forced continuous operation when tied to ground. High efficiency Burst Mode operation is enabled by either floating this pin or by tying this pin to $INTV_{CC}$. When driven with an external clock, an internal phase-locked loop will synchronize the phase and frequency of the internal oscillator to that of the incoming clock signal. During external clock synchronization, the LTC3601 will default to forced continuous operation.

PGOOD (Pin 2/Pin 16): Open-Drain Power Good Output Pin. PGOOD is pulled to ground when the voltage at the FB pin is not within 8% (typical) of the internal 0.6V reference. PGOOD becomes high impedance once the voltage at the FB pin returns to within ±5% (typical) of the internal reference.

SW (Pins 3, 4/Pins 1, 2): Switch Node Output Pin. Connect this pin to the SW side of the external inductor. The normal operation voltage swing of this pin ranges from ground to PV_{IN}.

BOOST (Pin 6/Pin 5): Boosted Floating Driver Supply Pin. The (+) terminal of the external bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to PV_{IN} + $INTV_{CC}$.

$INTV_{CC}$ (Pin 7/Pin 6): Internal 3.3V Regulator Output Pin. This pin should be decoupled to PGND with a low ESR ceramic capacitor of 1µF or more.

V_{ON} (Pin 8/Pin 7): On-Time Voltage Input Pin. This pin sets the voltage trip point for the on-time comparator. Connect this pin to the regulated output to make the on-time proportional to the output voltage when $V_{OUT} \leq 6V$. If $V_{OUT} > 6V$, switching frequency may become higher than the set frequency. The pin impedance is normally 180kΩ.

SGND (Pin 9/Exposed Pad Pin 17): Signal Ground Pin. This pin should have a low noise connection to reference ground. The feedback resistor network, external compensation network and RT resistor should be connected to this ground. In the MSE package, the exposed pad must be soldered to the PCB to provide a good thermal contact to the PCB.

RT (Pin 10/Pin 8): Oscillator Frequency Program Pin. Connect an external resistor, between 80k to 400k, from this pin to SGND to program the LTC3601 switching frequency from 800kHz to 4MHz. When RT is tied to $INTV_{CC}$, the switching frequency will default to 2MHz.

FB (Pin 11/Pin 9): Output Voltage Feedback Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage.

ITH (Pin 12/Pin 10): Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

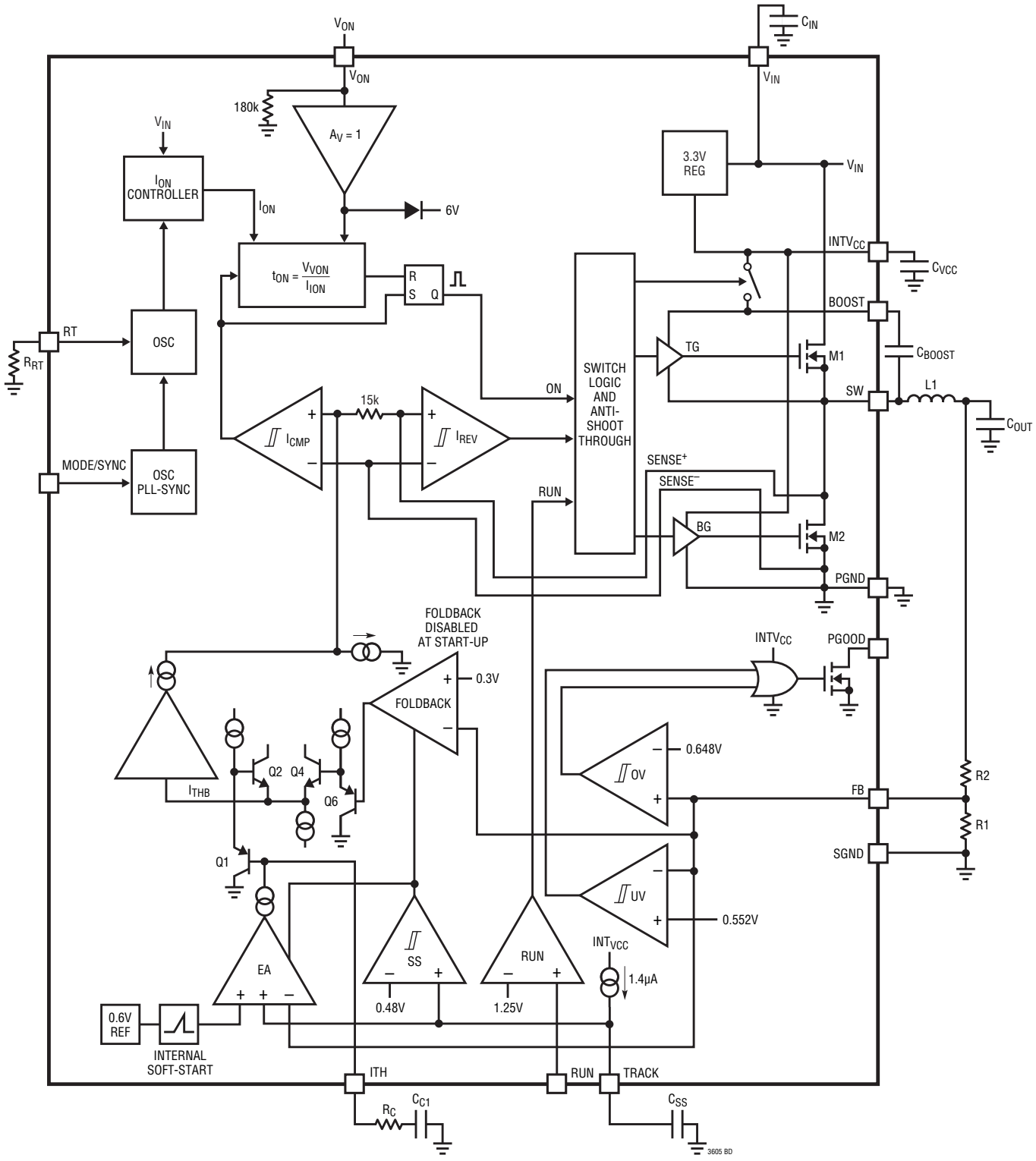
TRACK (Pin 13/Pin 11): Output Voltage Tracking and Soft-Start Input Pin. Forcing a voltage below 0.6V on this pin overrides the internal reference input to the error amplifier. The LTC3601 will servo the FB pin to the TRACK voltage under this condition. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull-up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting an external capacitor between this pin and ground. See Applications Information section for more details.

RUN (Pin 14/Pin 12): Regulator Enable Pin. Enables chip operation by applying a voltage above 1.25V. A voltage below 1V on this pin places the part into shutdown. Do not float this pin.

V_{IN} (Pins 15, 16/Pins 13, 14): Main Power Supply Input Pins. These pins should be closely decoupled to PGND with a low ESR capacitor of 10µF or more.

PGND (Exposed Pad Pin 17/Pins 3, 4): Power Ground Pin. The (–) terminal of the input bypass capacitor, C_{IN}, and the (–) terminal of the output capacitor, C_{OUT}, should be tied to this pin with a low impedance connection. In the QFN package the exposed pad must be soldered to the PCB to provide low impedance electrical contact to ground and good thermal contact to the PCB.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The LTC3601 is a current mode, monolithic, step-down regulator capable of providing up to 1.5A of output current. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a constant switching frequency. Part operation is enabled by raising the voltage on the RUN pin above 1.25V nominally.

Main Control Loop

In normal operation the internal top power MOSFET is turned on for a fixed interval determined by an internal one-shot timer ("ON" signal in the Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, I_{CMP}, trips, thus restarting the one-shot timer and initiating the next cycle. The inductor current is monitored by sensing the voltage drop across the SW and PGND nodes of the bottom power MOSFET. The voltage at the ITH pin sets the I_{CMP} comparator threshold corresponding to the inductor valley current. The error amplifier EA adjusts this ITH voltage by comparing an internal 0.6V reference to the feedback signal, V_{FB}, derived from the output voltage. If, for example, the load current increases, the feedback voltage will decrease relative to the internal 0.6V reference. The ITH voltage then rises until the average inductor current matches that of the load current.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-locked loop servos the switching regulator on-time to track the internal oscillator edge and force a constant switching frequency. A clock signal can be applied to the SYNC/MODE pin to synchronize the switching frequency to an external source. The regulator defaults to forced continuous operation once the clock signal is applied.

At low load currents the inductor current can drop to zero or become negative. If the LTC3601 is configured for Burst Mode operation, this inductor current condition is detected by the current reversal comparator, I_{REV}, which in turn shuts off the bottom power MOSFET and places the part into a low quiescent current sleep state resulting in discontinuous operation and increased efficiency at low load currents. Both power MOSFETs will remain off with the part in sleep and the output capacitor supplying the load current until the ITH voltage rises sufficiently to initiate another cycle. Discontinuous operation is disabled by tying the MODE/SYNC pin to ground placing the LTC3601 into forced continuous mode. During forced continuous mode, continuous synchronous operation occurs regardless of the output load current.

"Power Good" Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This condition is released once regulation within a 5% window is achieved. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3601 PGOOD falling edge includes a filter time of approximately 40µs.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3601 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 17.5V, the regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 16.5V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

Short-Circuit Protection

Foldback current limiting is provided in the event the output is inadvertently shorted to ground. During this condition the internal current limit (I_{LIM}) will be lowered to approximately one-third its normal value. This feature reduces the heat dissipation in the LTC3601 during short-circuit conditions and protects both the IC and the input supply from any potential damage.

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A general LTC3601 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and begins with the selection of the inductor L. Once the inductor is chosen, the input capacitor, C_{IN}, the output capacitor, C_{OUT}, the internal regulator capacitor, C_{INTVCC}, and the boost capacitor, C_{BOOST}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, track/soft-start, externally programmed oscillator frequency and PGOOD.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, f_O, of the LTC3601 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{RT} = \frac{3.2\ E11}{f_O}$$

where R_{RT} is in Ω and f_O is in Hz.

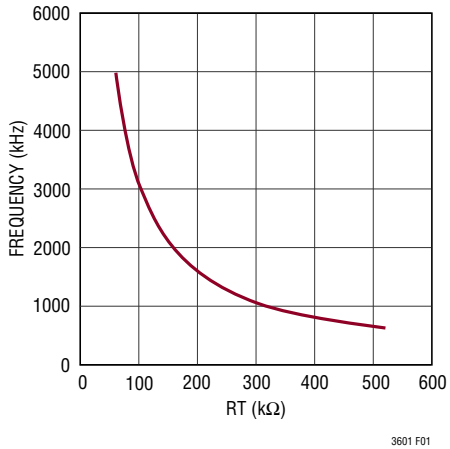

Figure 1. Switching Frequency vs RT

Connecting the RT pin to $INTV_{CC}$ will default the converter to f_O = 2MHz; however, this switching frequency will be more sensitive to process and temperature variations than when using a resistor on RT (see Typical Performance Characteristics).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_L = inductor ripple current, f = operating frequency and L = inductor value. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point for setting the ripple current is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee the ripple current does not exceed a specified maximum the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

However, the inductor ripple current must not be so large that its valley current level exceeds the negative current limit of –1.2A (typical) when the circuit is operating in forced continuous mode. If the inductor current trough reaches the negative current limit while the part is in forced continuous mode operation, V_{OUT} may charge up to above its target regulation voltage. In such instances, choose a larger inductor value to reduce the ripple current. The alternative is to reduce the inductor ripple current by decreasing the R_T resistor value, which will increase the switching frequency.

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Once the value for L is known the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value but is very dependent on the inductance selected. As the inductance increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire leading to increased copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate "hard," meaning the inductance collapses abruptly when the peak design current is exceeded. This collapse will result in an abrupt increase in inductor ripple current, so it is important to ensure the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, Coilcraft, TDK and Wurth Electronik. Table 1 gives a sampling of available surface mount inductors.

Table 1. Inductor Selection Table

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Würth Electronik WE-PD2 Typ MS Series				
0.56	9.5	6.5	5.2 × 5.8	2
0.82	14	5.4		
1.2	21	4.8		
1.7	27	4		
2.2	36	3.6		
Vishay IHLP-2020BZ-01 Series				
0.47	8.8	11.5	5.2 × 5.5	2
0.68	12.4	10		
1	20	7		
2.2	50.1	4.2		
Toko DE3518C Series				
0.56	24	3.3	3.5 × 3.7	1.8
1.2	30	2.4		
1.7	35	2.1		
Sumida CDRH2D18/HP Series				
0.56	33	3.7	3.2 × 3.2	2
0.82	39	2.9		
1.1	43	2.5		
Cooper SD18 Series				
0.47	20.1	3.58	5.5 × 5.5	1.8
0.82	24.7	3.24		
1.2	29.4	2.97		
1.5	34.5	2.73		
2.2	39.8	2.55		
Coilcraft LPS4018 Series				
0.56	30	4.8	4 × 4	1.7
1	40	2.8		
2.2	70	2.7		
TDK VLS252012 Series				
0.47	56	3.3	2.5 × 2	1.2
1	88	2.4		
1.5	126	2		
2.2	155	1.8		

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ equals the maximum average output current. This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor or choose a capacitor rated at a higher temperature than required.

Several capacitors may be paralleled to meet the requirements of the design. For low input voltage applications sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3601 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is primarily determined by the effective series resistance (ESR) that is required to minimize

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voltage ripple and load step transients. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiple capacitors in parallel.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in small case sizes. Their high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors choose the X5R or X7R dielectric formulations. These dielectrics provide the best temperature and voltage characteristics for a given value and size.

$INTV_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator produces a 3.3V supply voltage used to power much of the internal LTC3601 circuitry including the power MOSFET gate drivers. The $INTV_{CC}$ pin connects to the output of this regulator and must have a minimum of 1µF of decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the $INTV_{CC}$ and PGND pins to provide the transient currents required by the LTC3601. The user may connect a maximum load current of 5mA to this pin but must take into account the increased power dissipation and die temperature that results. Furthermore, this supply is intended only to supply additional DC load currents as desired and not intended to regulate large transient or AC behavior this may impact LTC3601 operation.

Boost Capacitor

The boost capacitor, C_{BOOST}, is used to create a voltage rail above the applied input voltage V_{IN}. Specifically, the boost capacitor is charged to a voltage equal to approximately $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V_{IN} + 3.3V. For most applications a 0.1µF ceramic capacitor will provide adequate performance.

Output Voltage Programming

The LTC3601 will adjust the output voltage such that V_{FB} equals the reference voltage of 0.6V according to:

$$V_{OUT} = 0.6V \left(1 + \frac{R1}{R2} \right)$$

The desired output voltage is set by appropriate selection of resistors R1 and R2 as shown in Figure 2. Choosing large values for R1 and R2 will result in improved efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the FB node. Care should be taken to route the FB line away from any noise source, such as the SW line.

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To improve the frequency response of the main control loop a feedforward capacitor, C_F, may be used as shown in Figure 2.

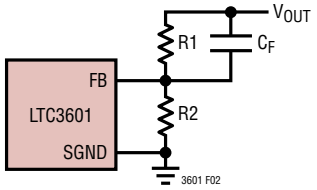

Figure 2. Optional Feedforward Capacitor

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3601 can turn on the bottom power MOSFET, trip the current comparator and turn the power MOSFET back off. This time is typically 40ns. For the controlled on-time current mode control architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{(MAX)} = 1 - \left(f \bullet t_{OFF(MIN)}\right)$$

where f is the switching frequency and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - \left(f \bullet t_{OFF(MIN)}\right)}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{(MIN)} = \left(f \bullet t_{ON(MIN)}\right)$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases, and high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor and Capacitor Selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

Internal/External Loop Compensation

The LTC3601 provides the option to use a fixed internal loop compensation network to reduce both the required external component count and design time. The internal loop compensation network can be selected by connecting the ITH pin to the $INTV_{CC}$ pin. To ensure stability, it is recommended that the output capacitance be at least 47µF when using internal compensation. Alternatively, the user may choose specific external loop compensation components to optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the ITH pin.

Suggested compensation component values are shown in Figure 3. For a 2MHz application, an R-C network of 220pF and 13kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 10pF bypass capacitor on the ITH pin is recommended for the purposes of filtering out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor C_F can be added to improve the high frequency response, as previously shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R1 which improves the phase margin.

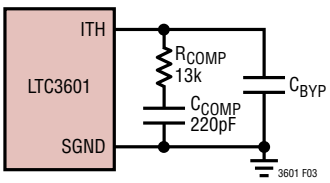

Figure 3. Compensation Components

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Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time, and settling behavior at this test point reflect the system's closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated by observing the percentage of overshoot seen at this pin. The ITH external components shown in Figure 3 will provide an adequate starting point for most applications. The series R-C filter sets the pole-zero loop compensation. The values can be modified slightly, from approximately 0.5 to 2 times their suggested values, to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current with a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop. As a result, the standard second order overshoot/DC ratio cannot be used to estimate phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76. As shown in Figure 2 a feedforward capacitor, C_F, may be added across feedback resistor R1 to improve the high frequency response of the system. Capacitor C_F provides phase lead by creating a high frequency zero with R1.

In some applications severe transients can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this output droop if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection and soft-start functions.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Connecting this pin to $INTV_{CC}$ enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is pulled to ground, forced continuous mode operation is selected creating the lowest fixed output ripple at the expense of light load efficiency.

The LTC3601 will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place the LTC3601 into forced continuous mode operation.

Output Voltage Tracking and Soft-Start

The LTC3601 allows the user to control the output voltage ramp rate by means of the TRACK pin. From 0V to 0.6V the TRACK pin will override the internal reference input to the error amplifier forcing regulation of the feedback voltage to that seen at the TRACK pin. When the voltage at the TRACK pin rises above 0.6V, tracking is disabled and the feedback voltage will be regulated to the internal reference voltage.

The voltage at the TRACK pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4µA pull-up current on TRACK to implement

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a soft-start function by connecting a capacitor from the TRACK pin to ground. The relationship between output rise time and TRACK capacitance is given by:

$$t_{SS} = 430{,}000 \times C_{TRACK}$$

A default internal soft-start timer forces a minimum soft-start time of 400µs by overriding the TRACK pin input during this time period. Hence, capacitance values less than approximately 1000pF will not significantly affect soft-start behavior.

When using the TRACK pin, the regulator defaults to Burst Mode operation until the output exceeds 80% of its final value (V_{FB} > 0.48V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value (as it may when tracking down, for instance), the regulator will automatically switch to Burst Mode operation to prevent inductor saturation and improve TRACK pin accuracy.

Output Power Good

The PGOOD output of the LTC3601 is driven by a 15Ω (typical) open-drain pull-down device. This device will be turned off once the output voltage is within 5% (typical) of the target regulation point allowing the voltage at PGOOD to rise via an external pull-up resistor (100k typical). If the output voltage exits a 8% (typical) regulation window around the target regulation point the open-drain output will pull down with 15Ω output resistance to ground, thus dropping the PGOOD pin voltage. A filter time of 40µs (typical) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. As a result, the output voltage must be within the target regulation window of 5% for 40µs before the PGOOD pin is pulled high. Conversely, the output voltage must exit the 8% regulation window for 40µs before the PGOOD pin pulls to ground (see Figure 4).

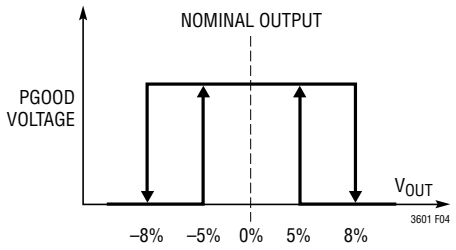

Figure 4. PGOOD Pin Behavior

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources account for the majority of the losses in the LTC3601: 1) I^2R loss, 2) switching losses and quiescent current loss, 3) transition losses and other system losses.

1. I^2R loss is calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current will flow through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET's $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

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The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R loss:

"I^2R LOSS" = $I_{OUT}^2 \cdot (R_{SW} + R_L)$

2. The internal LDO supplies the power to the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

   Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on the LTC3601 is approximately 1nC.

   To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by V_{IN}:

   $P_{LDO} = (I_{GATECHG} + I_Q) \bullet V_{IN}$

3. Other "hidden" losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3601 internal power devices switch quickly enough that these losses are not significant compared to other sources.

   Other losses, including diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3601 requires the exposed package backplane metal (PGND pin on the QFN, SGND pin on the MSOP package) to be well soldered to the PC board to provide good thermal contact. This gives the QFN and MSOP packages exceptional thermal properties, compared to other packages of similar size, making it difficult in normal operation to exceed the maximum junction temperature of the part. In many applications, the LTC3601 does not dissipate much heat due to its high efficiency and low thermal resistance package backplane. However, in applications in which the LTC3601 is running at a high ambient temperature, high input voltage, high switching frequency, and maximum output current, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off until temperature decreases approximately 10°C.

Thermal analysis should always be performed by the user to ensure the LTC3601 does not exceed the maximum junction temperature.

The temperature rise is given by:

$T_{RISE} = P_D\theta_{JA}$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

Consider the example in which an LTC3601EUD is operating with I_{OUT} = 1.5A, V_{IN} = 12V, f = 4MHz, V_{OUT} = 1.8V, and an ambient temperature of 70°C. From the Typical Performance Characteristics section the $R_{DS(ON)}$ of the top switch is found to be nominally 130mΩ while that of the bottom switch is nominally 100mΩ yielding an equivalent power MOSFET resistance R_{SW} of:

$R_{DS(ON)}TOP \bullet 1.8/12 + R_{DS(ON)}BOT \bullet 10.2/12 = 105m\Omega$.

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From the previous section, $I_{GATECHG}$ is ~4mA when f = 4MHz, and the spec table lists the typical I_Q to be 1mA. Therefore, the total power dissipation due to resistive losses and LDO losses is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet (I_{GATECHG} + I_Q)$$

$$P_D = (1.5)^2 \bullet (0.105) + 12V \bullet 5mA = 296mW$$

The QFN 3mm × 3mm package junction-to-ambient thermal resistance, θ_{JA}, is around 45°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.296 \bullet 45 + 70 = 83.3°C$$

which is well below the specified maximum junction temperature of 125°C.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3601.

1. Do the capacitors C_{IN} connect to V_{IN} and PGND as close to the pins as possible? These capacitors provide the AC current to the internal power MOSFETs and drivers. The (–) plate of C_{IN} should be closely connected to PGND and the (–) plate of C_{OUT}.
2. The output capacitor, C_{OUT}, and inductor L1 should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to PGND and the (–) plate of C_{IN}.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal, V_{FB}, should be routed away from noisy components and traces such as the SW line, and its trace length should be minimized. In addition, RT and the loop compensation components should be terminated to SGND.
4. Keep sensitive components away from the SW pin. The R_{RT} resistor, the feedback resistors, the compensation components, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor.
5. A ground plane is preferred, but if not available the signal and power grounds should be segregated with both connecting to a common, low noise reference point. The point at which the ground terminals of the V_{IN} and V_{OUT} bypass capacitors are connected makes a good, low noise reference point. The connection to the PGND pin should be made with a minimal resistance trace from the reference point.
6. Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside connection of the IC.

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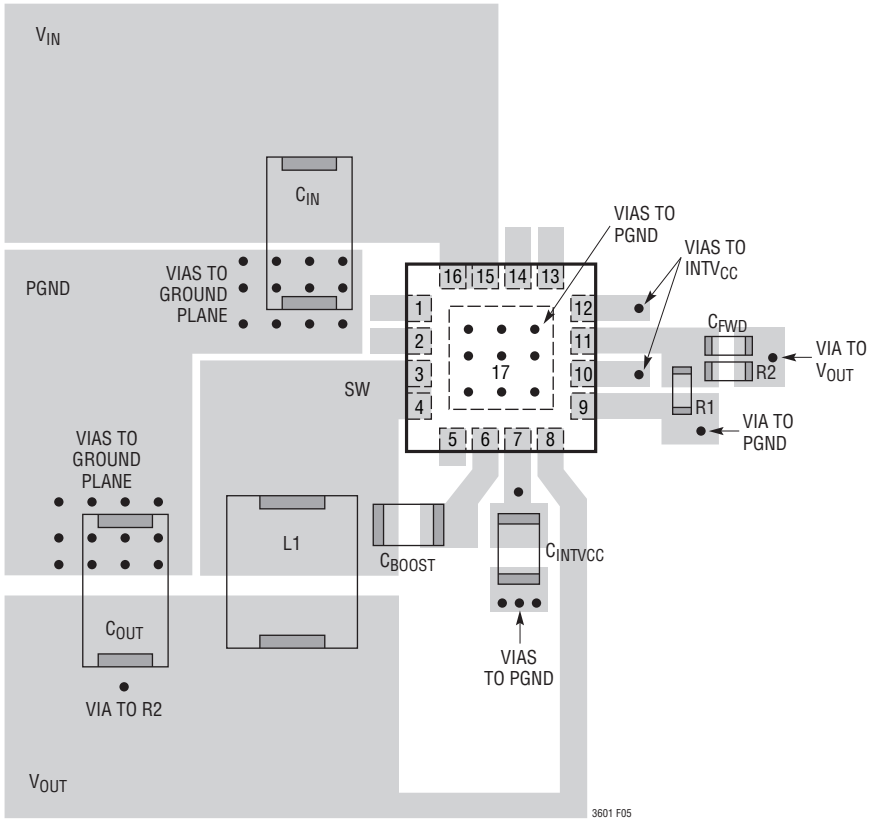


Figure 5. QFN Layout Example

APPLICATIONS INFORMATION

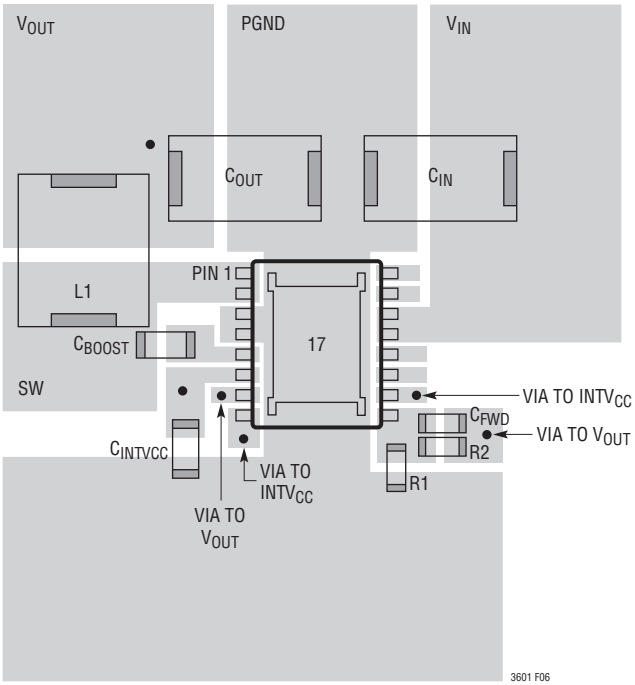


Figure 6. MSE Layout Example

APPLICATIONS INFORMATION

Design Example

As a design example, consider using the LTC3601 in an application with the following specifications:

V_{IN} = 12V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 1.5A, $I_{OUT(MIN)}$ = 10mA, f = 1MHz

Because efficiency is important at both high and low load currents, Burst Mode operation is selected.

First, the correct R_{RT} resistor value for 1MHz switching frequency must be chosen. Based on the equation discussed earlier, R_{RT} should be 324k.

Next, determine the inductor value for approximately 40% ripple current using:

$$L = \left(\frac{1.8V}{1MHz \bullet 600mA}\right)\left(1 - \frac{1.8V}{12V}\right) = 2.55\mu H$$

A standard value 2.2µH inductor will work well for this application.

Next, C_{OUT} is selected based on the required output transient performance and the required ESR to satisfy the output voltage ripple. For this design, a 22µF ceramic capacitor will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 1.5A\left(\frac{\sqrt{1.8V\left(12V - 1.8V\right)}}{12V}\right) = 0.54A$$

Decoupling the V_{IN} pins with a 22µF ceramic capacitor should be adequate for most applications. A 0.1µF boost capacitor should also work for most applications.

To save board space the I_{TH} pin is connected to the $INTV_{CC}$ pin to select an internal compensation network.

The PGOOD pin is connected to V_{IN} through a 100k resistor.

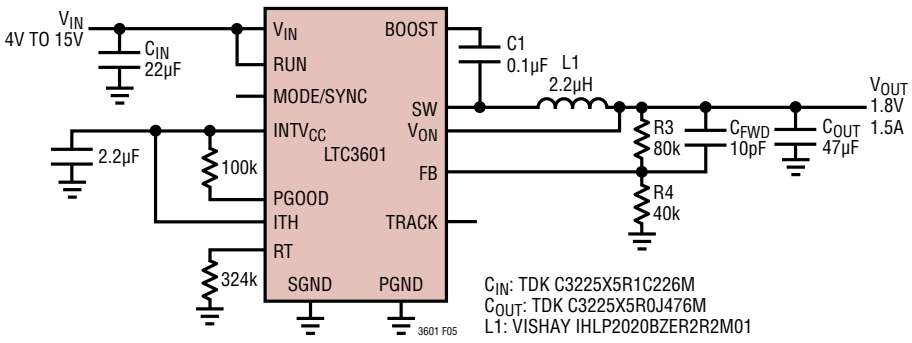
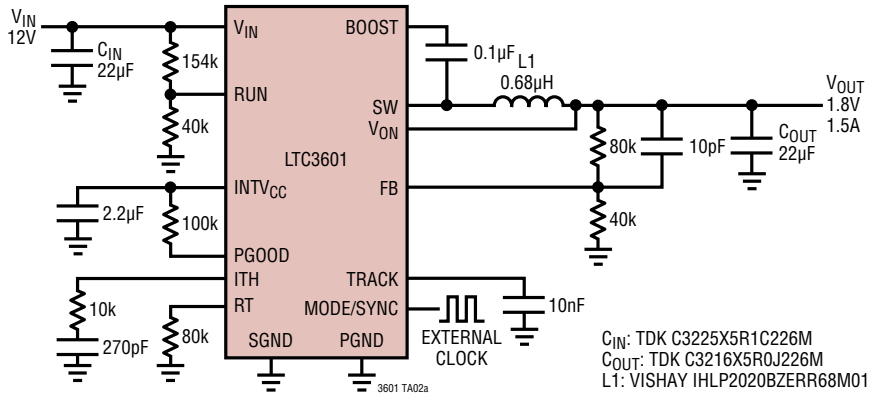


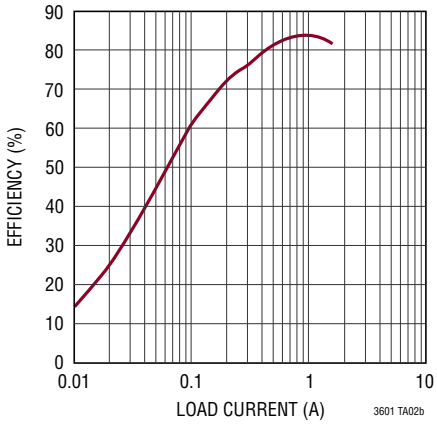
Figure 7. 1.8V, 1.5A Regulator at 1MHz

TYPICAL APPLICATIONS

12V Input to 1.8V Output at 4MHz Synchronized Frequency with 6V UVLO and 4.3ms Soft-Start

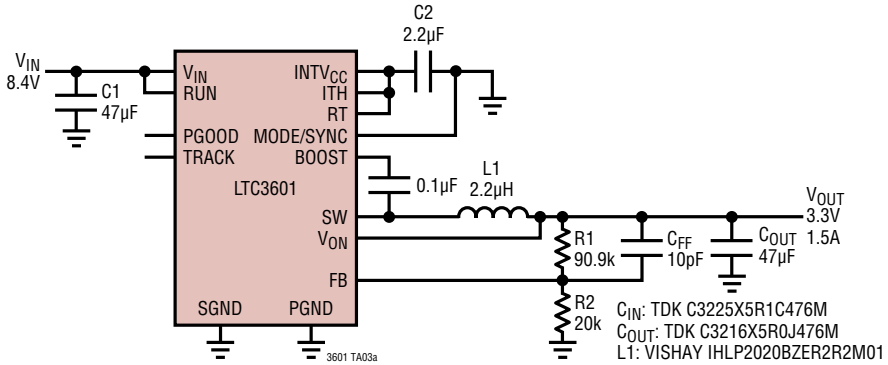


Efficiency vs Load Current

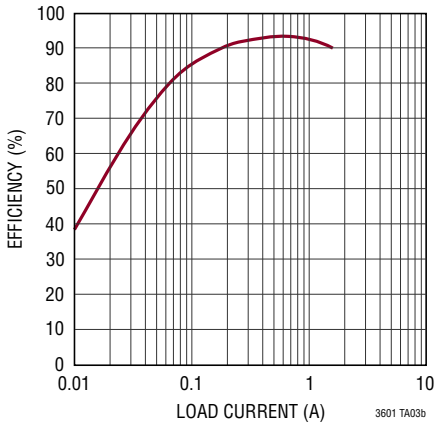


TYPICAL APPLICATIONS

8.4V Input to 3.3V Output at 2MHz Operating Frequency Using Forced Continuous Mode



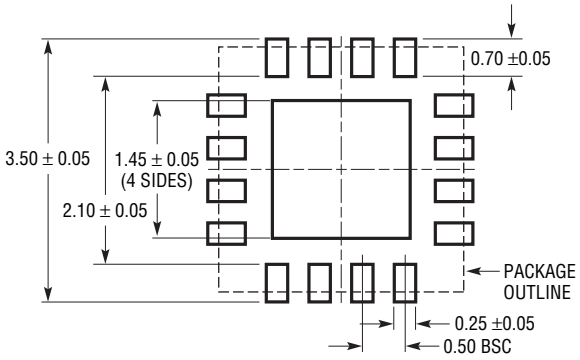
Efficiency vs Load Current



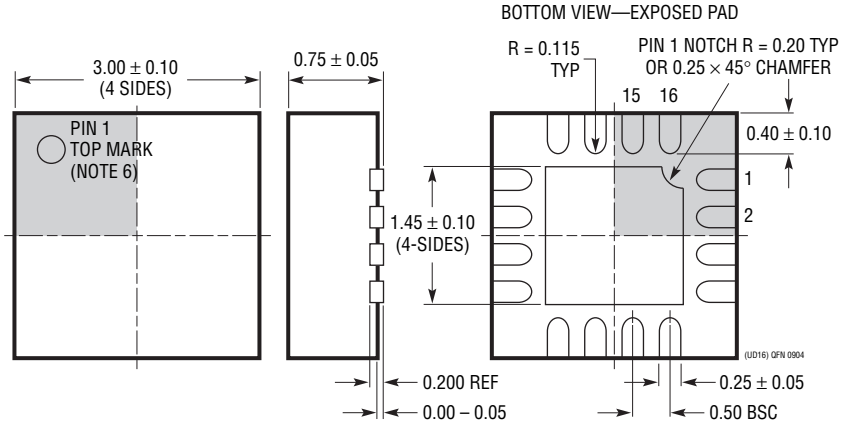
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

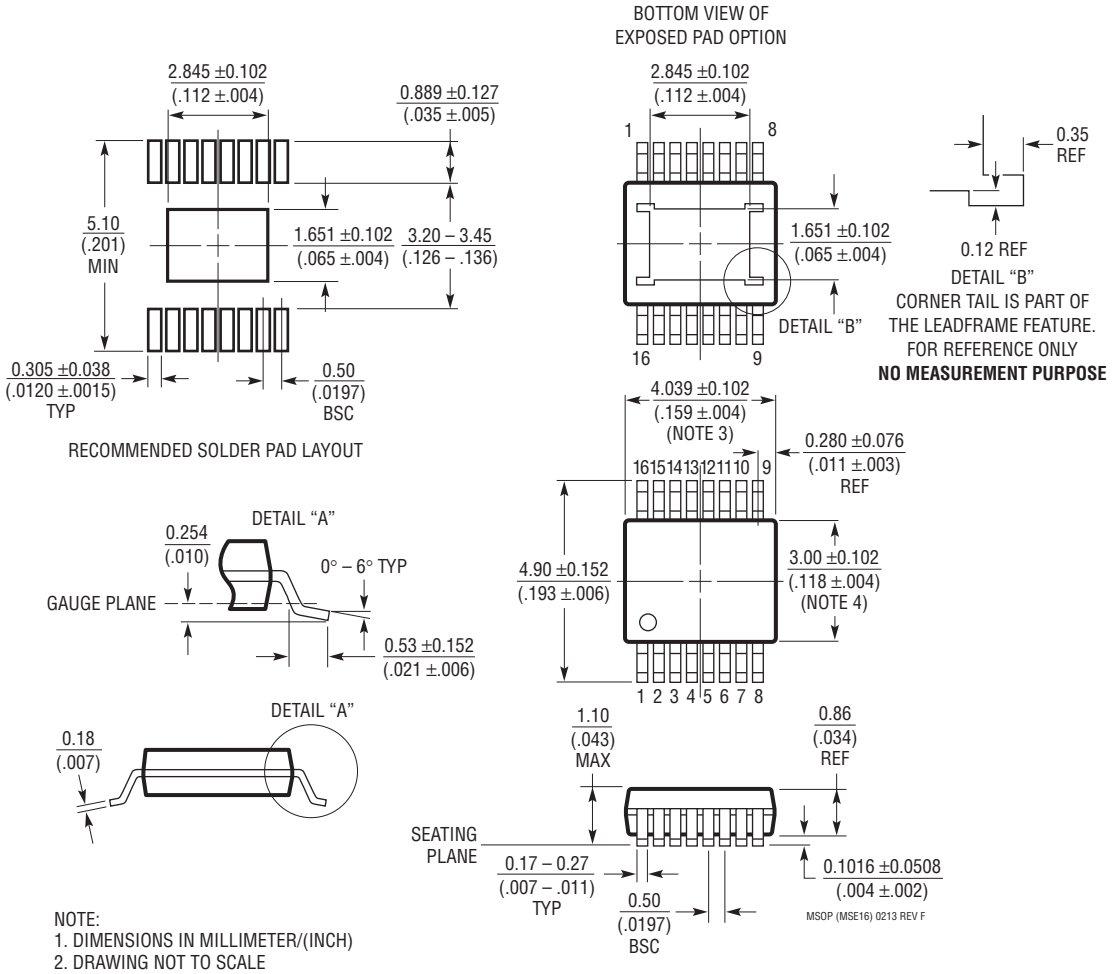


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



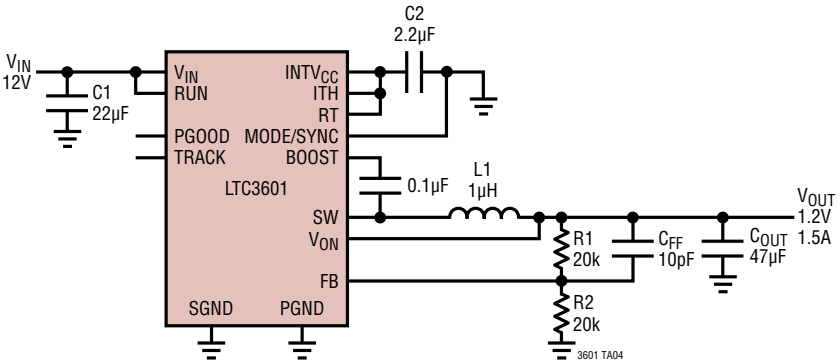
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/10	Changed Temperature Range for E-Grade to –40°C to 125°C in Order Information Sections	2
		Updated Note 2	3
		Updated Pin Functions	7
		Updated Functional Block Diagram	8
		Updated Equation in Applications Information Section	11, 15
		Updated Related Parts	26
B	11/11	Changed Units from mV to V on the V_{F_TRACK} specification	3
		Updated Axis labels on graphs G17 and G18	6
C	08/15	Added Negative Valley Switch Current Limit	3
		Modified Inductor Selection section	10

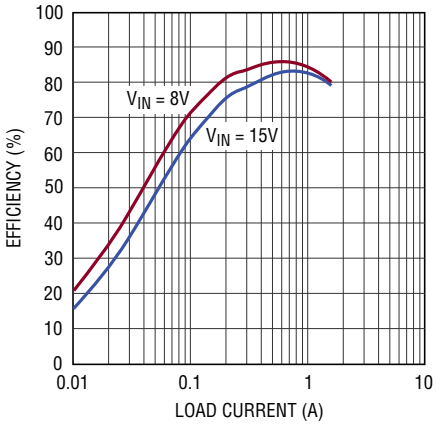
TYPICAL APPLICATION

1.2V Output at 2MHz Operating Frequency



C_{IN}: TDK C3225X5R1C226M
C_{OUT}: TDK C3225X5R0J476M
L1: VISHAY IHLP2020BZER1R0M01

Efficiency vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3602	10V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 10V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, TSSOP-16E
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14mA, 3mm × 3mm QFN-16 and MSOP-16E Packages
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3610	24V, 12A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 24V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN-64
LTC3611	32V, 10A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 32V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN-64

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